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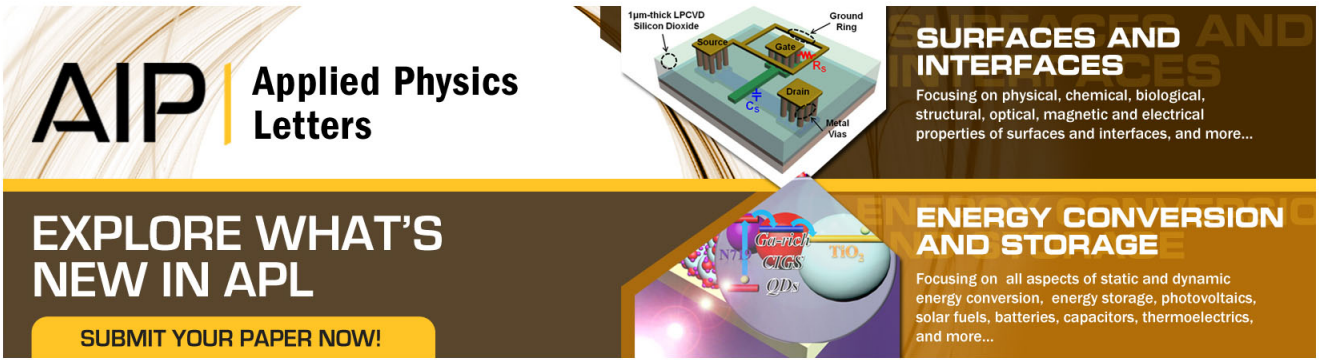

High quality single-crystal germanium-on-insulator on bulk Si substrates based on multistep lateral over-growth with hydrogen annealing

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Germanium-on-insulator (GOI) is desired for high performance metal-oxide-semiconductor transistors and monolithically integrated optoelectronics. We demonstrate a promising approach to achieve single-crystal defect-free GOI by using lateral over-growth through SiO_2 window. The dislocations due to the lattice mismatch are effectively terminated and reduced in SiO_2 trench by selective area heteroepitaxy combined with hydrogen annealing. Low defect density of 4×10^6 cm^{-2} and low surface roughness of 0.7 nm (root-mean-square) on GOI are confirmed by plan-view transmission electron microscopy and atomic force microscopy analysis. In addition, the excellent metal-semiconductor-metal diode electrical characteristics fabricated on this GOI confirm Ge crystal quality. The selectively grown GOI structure can provide the monolithic integration of SiGe based devices on a Si very large scale integration (VLSI) platform. © *2010 American Institute of Physics*.
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Germanium has been considered as a promising material for high performance complementary metal-oxide-semiconductor (CMOS) transistors and optoelectronic applications as it offers much higher and symmetric carrier mobility[1–3] and smaller optical band gap ideal for 1.3–1.5 μm wavelength commonly used in telecommunication.[4] Germanium-on-insulator (GOI) can specially provide high performance MOS field-effect transistors by high-speed operation as well as low parasitic capacitance and immunity for short channel effects. Low-leakage junction current by thin-body GOI is also another benefit for channel materials with smaller band gap.[5,6] Even more research efforts are directed toward the realization of on-chip optical signaling using Ge-based devices. There has been a surge in interest in SiGe based optoelectronics such as near IR detectors,[7–9] Ge-based integrated optical modulators,[10,11] and so on. The marriage of microelectronics to high performance photonics requires precise control and process compatibility. It is hence crucial to be able to grow high quality SiGe layers selectively on Si. For GOI structures, currently, many techniques such as oxidation-induced Ge condensation,[12] laser annealing,[13,14] solid-phase crystallization,[15,16] metal-induced lateral crystallization,[17] bonding,[18] and lateral epitaxial growth[19] have been introduced. However, these techniques to obtain GOI structures can be very complicated and have difficulty in achieving high-quality Ge films. In addition, the monolithic integration with Si based CMOS technology seems to be much more difficult. In other material, such as GaN, lateral overgrowth technique has been demonstrated to effectively reduce dislocation densities on GaN films and was used to fabricate very high performance light emitting diodes and laser diodes.[20–22]

In this paper, we demonstrate the lateral overgrowth of germanium on a SiO_2 layer with multistep lateral overgrowth with hydrogen annealing (MLHA) technique. This MLHA technique yields Ge layers with very low dislocation density and surface roughness as confirmed by transmission electron microscope (TEM) analysis, and atomic force microscope (AFM) surface morphology studies. In addition, metal-semiconductor-metal (MSM) diode electrical characteristics are shown to confirm Ge crystal quality on SiO_2.

A SiO_2 layer was thermally grown on p-type (100) Si substrate at 1100 °C that finally became the insulator layer of the GOI structure. The SiO_2 film was then patterned by dry-etching followed by wet-etching. These etched vias became the growth windows for selective Ge epitaxy. The starting surface is very critical in epitaxy for single-crystal growth; therefore, the samples were etched in 50:1 (H_2O:HF) for 30 s and immediately loaded into an Applied Materials Centura epitaxial reactor. A hydrogen bake at 1000 °C was carried out to ensure that no native oxide remained on the Si surface between SiO_2 walls. In order to increase the resulting films quality, a very thin Si epilayer was first grown for 90 s at 700 °C with dichlorosilane as the reaction species.

Ge growth on Si is surface reaction limited below 450 °C and is mass transport limited above.[23] Therefore, low growth temperatures and pressures provide better selectivity between Si and SiO_2. The reaction temperature was found to influence the growth rates of different crystal directions, as reported elsewhere.[24] At 400 °C, ⟨100⟩ normal direction was dominant at 30 nm/min compared to 3 nm/min in ⟨113⟩ direction. This resulted in facet formation with {113} surfaces. At elevated temperatures such as 600 °C, growth rates for ⟨100⟩ and ⟨113⟩ directions were 60 nm/min and 12 nm/min, respectively. Therefore, a careful design of the growth con-

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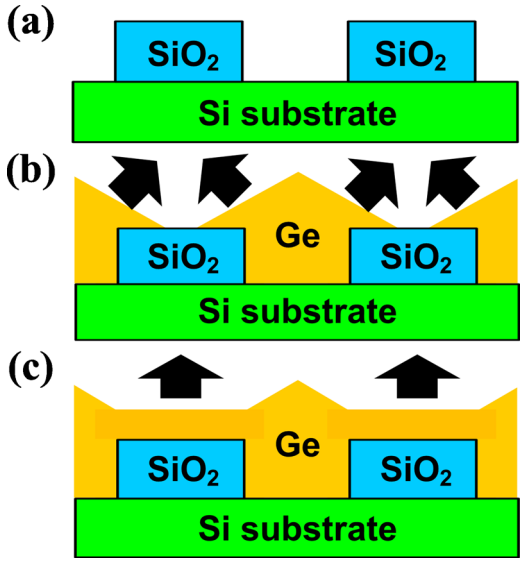

FIG. 1. (Color online) Illustration (a) of selective Ge growth at 400 °C on Si through openings in the SiO_2 film. (b) Illustration of the growth mechanism at 400 °C before the films coalesce, (c) growth at 600 °C after coalescence.

ditions and a trade off between nucleation/selectivity and growth rate is required to achieve high quality GOI virtual substrates. Figure 1 shows the schematic of the lateral overgrowth Ge process. As shown Fig. 1(a), an initial low-temperature growth is performed for higher $Si-SiO_2$ selectivity and reduced surface roughness. Once Ge layer becomes pyramidlike shape in the SiO_2 trench, ⟨311⟩ direction growth becomes dominant before coalescences in Fig. 1(b). After the coalescence happens, ⟨100⟩ direction growth starts at the valley where two Ge growth fronts meet at specific condition. As shown in Fig. 1(c), due to a higher growth rate of ⟨100⟩ direction compared to that of ⟨311⟩ direction, the valley is quickly filled up and ⟨100⟩ growth is dominant.

The initial Ge layer was grown at 400 °C with a partial pressure of 8 Pa. Temperature in the chamber was raised to 825 °C and the sample was annealed for 30 min in H_2 ambient. This step is crucial to allow for surface reconstruction, reduce dislocation density and surface roughness.[23,25] An

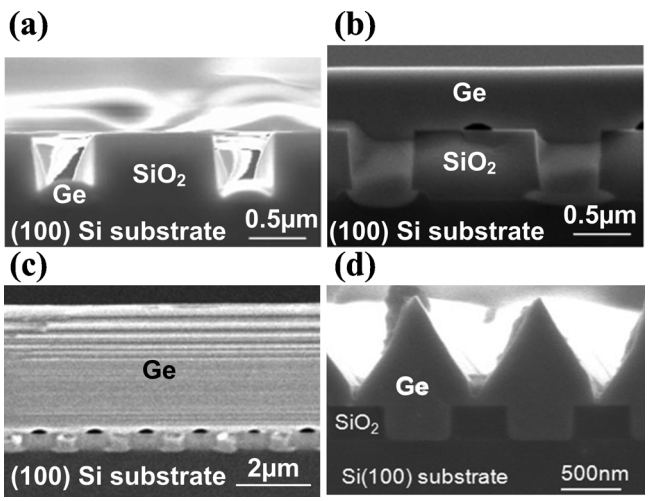

FIG. 2. Cross-sectional SEM images of the film after (a) growth at 400 °C, (b) growth at 400 °C followed by 15 min at 600 °C, (c) growth at 400 °C followed by 35 min at 600 °C, and (d) growth at 400 °C for 1 h.

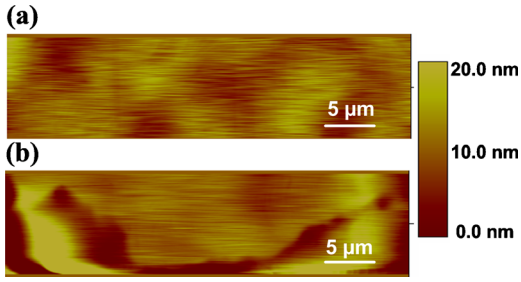

FIG. 3. (Color online) AFM scan images of 40×10 μm^2 of the resulting thick film after low-temperature (400 °C) and high-temperature (600 °C) growth (a) with and (b) without intermediate H_2 anneal steps.

scanning electron microscopy (SEM) image of the sample after this step is shown in Fig. 2(a). After the coalescence, an additional growth step was performed at 600 °C for 15 min followed by H_2 annealing at 825 °C, where the valley was filled up due to fast ⟨100⟩ direction growth. However, as shown in Fig. 2(d), ⟨100⟩ direction growth does not start at the valley after the coalescence of Ge films at 400 °C additional growth step. Figure 2(b) shows the resulting lateral over-lateral growth with the 400 °C and 600 °C growth temperature combination. The overall Ge layer thickness can be increased by longer growth at 600 °C as demonstrated in Fig. 2(c) for a growth time of 35 min.

Large surface roughness and dislocation density are observed on as-grown samples as a result of the 4.2% lattice mismatch between Si and Ge. The surface roughness reduction by annealing in hydrogen ambient at 825 °C is attributed to hydrogen-mediated Ge diffusion and the reconstruction of the surface.[23] Figure 3 shows 40×10 μm^2 AFM scan images for two lateral overgrowth Ge films grown without hydrogen annealing and with MLHA. The surface of the sample with no annealing was significantly smoothened with MLHA. A very low rms surface roughness of 0.7 nm was achieved in MLHA GOI samples down from 3.5 nm for unannealed GOI films.

GOI film quality was investigated by TEM analysis. TEM images in Fig. 4 show very high quality Ge layers obtained on SiO_2. Ge film grows selectively through a 500 nm wide window in the SiO_2 layer. Defects were found only in the first 60 nm thick region from the Ge and Si interface. Previous efforts to obtain high quality epilayers on

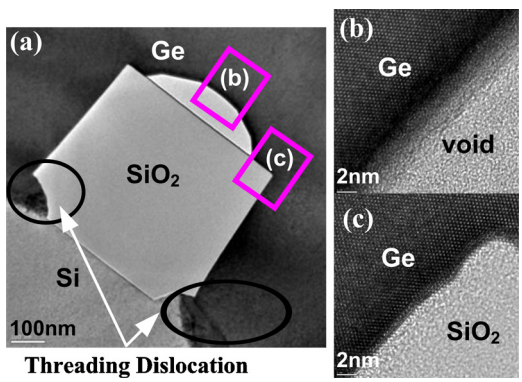

FIG. 4. (Color online) (a) Cross sectional TEM (XTEM) image of grown Ge film and the SiO_2 mesa block. Defects and dislocations are in close vicinity of the Ge–Si interface while the rest of the film has very low defect density. [(b) and (c)] High resolution XTEM images of the Ge film on top of the SiO_2 mesa and the void, showing defect free GOI layers.

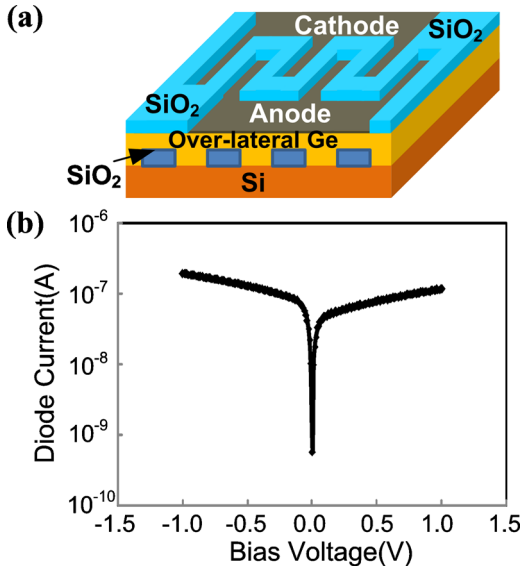

FIG. 5. (Color online) (a) Cross-section of MSM diode fabricated on over-lateral grown Ge layer. (b) Current vs voltage characteristics of metal-semiconductor (Ti–Ge) Schottky diode on over-lateral grown GOI, both forward and reverse bias regions.

Si required a 500 nm or thicker buffer layers to confine the defects and dislocations.[10,26] The hydrogen annealing technique reported in this work increases the surface mobility of Ge atoms leading dislocations to glide to Ge/SiO_2. In other word, the SiO_2 sidewalls provide sinks for the dislocations. Once the Ge film thickness exceeds the height of the SiO_2 trench, the lateral overgrowth of the film results in extremely single-crystal GOI layer. Owing to MLHA, the lateral overgrown Ge layer shows very low defect density, having a threading dislocation density count of $\sim 4 \times 10^6$ cm^{-2} based on the plan view TEM analysis. Figures 4(b) and 4(c) also show no visible defect where the growth fronts join. This is attributed to dislocation trapping within SiO_2 trenches.

In order to confirm the high crystal quality of Ge layer over-laterally grown on SiO_2 electrically, we fabricated simple MSM diode with interdigitated electrode width (5 μm) and spacing (5 μm) on the top of the over-lateral grown Ge layer. A 200 nm thick low-temperature chemical-vapor-deposited oxide layer was deposited at 400 °C for the purpose of surface passivation and isolation. This oxide layer was lithographically patterned and HF-etched, followed by metal electrode e-beam evaporation and photoresist lift-off process. Figure 5(a) illustrates a schematic diagram of the final structure. 15 nm thick Ti was used for controlling work function as well as achieving good adhesion, and then it was topped with 35 nm thick Au. Figure 5(b) presents the electrical current-voltage (I-V) characteristic of MSM (Ti–Ge–Ti) diode. Therefore, high quality Ge layer introduces low leakage current.[27] Back-to-back Schottky diode behavior and low leakage current of 1.18×10^{-7} A at 1 V as shown in Fig. 5 confirms the excellent Ge crystal quality of over-lateral grown GOI substrate.

In conclusion, we have demonstrated very high quality and defect free GOI with MLHA. The multistep 400/600 °C growth mechanism achieves single-crystal GOI The MLHA. This MLHA technique yields Ge layers with very low dislocation density and surface roughness. Such an approach promises the integration of SiGe based devices on a Si very large scale integration (VLSI) platform.

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[1]C. O. Chui, H. Kim, D. Chi, B. B. Triplett, P. C. McIntyre, and K. C. Saraswat, Tech. Dig. - Int. Electron Devices Meet. **2002**, 441.
[2]C. H. Lee, T. Nishimura, N. Saido, K. Nagashio, K. Kita, and A. Toriumi, Tech. Dig. - Int. Electron Devices Meet. **2009**, 457.
[3]H.-Y. Yu, M. Ishibashi, J.-H. Park, M. Kobayashi, and K. C. Saraswat, IEEE Electron Device Lett. **30**, 675 (2009).
[4]K. Saraswat, D. Kim, T. Krishnamohan, D. Kuzum, A. Okyay, A. Pethe, and H.-Y. Yu, ECS Trans. **16**(10), 3 (2008).
[5]S.-I. Takagi, Dig. Tech. Pap. - Symp. VLSI Technol. **2003**, 115.
[6]T. Maeda, K. Ikeda, S. Nakaharai, T. Tezuka, N. Sugiyama, Y. Moriyama, and S. Takagi, Thin Solid Films **508**, 346 (2006).
[7]M. Oehme, J. Werner, E. Kasper, M. Jutzi, and M. Berroth, Appl. Phys. Lett. **89**, 071117 (2006).
[8]D. Ahn, C. Hong, J. Liu, W. Giziewicz, M. Beals, and L. C. Kimerling, Opt. Express **15**, 3916 (2007).
[9]H.-Y. Yu, S. Ren, W. S. Jung, A. K. Okyay, D. A. B. Miller, and K. C. Saraswat, IEEE Electron Device Lett. **30**, 1161 (2009).
[10]Y. H. Kuo, Y. Lee, Y. Ge, S. Ren, J. E. Roth, T. I. Kamins, D. A. B. Miller, and J. S. Harris, Nature (London) **437**, 1334 (2005).
[11]O. Fidaner, A. K. Okyay, J. E. Roth, R. K. Schaevitz, Y. H. Kuo, K. C. Saraswat, J. S. Harris, and D. A. B. Miller, IEEE Photonics Technol. Lett. **19**, 1631 (2007).
[12]S. Nakaharai, T. Tezuka, N. Sugiyama, Y. Moriyama, and S. Takagi, Appl. Phys. Lett. **83**, 3516 (2003).
[13]H. Watakabe, T. Sameshima, H. Kanno, T. Sadoh, and M. Miyao, J. Appl. Phys. **95**, 6457 (2004).
[14]W. Yeh, H. Chen, H. Huang, C. Hsiao, and J. Jeng, Appl. Phys. Lett. **93**, 094103 (2008).
[15]I. Tsunoda, A. Kenjo, T. Sadoh, and M. Miyao, Appl. Surf. Sci. **224**, 231 (2004).
[16]C. Y. Tsao, J. W. Weber, P. Campbell, P. I. Widenborg, D. Song, and M. A. Green, Appl. Surf. Sci. **255**, 7028 (2009).
[17]J.-H. Park, P. Kapur, H. Peng, and K. C. Saraswat, Appl. Phys. Lett. **91**, 143107 (2007).
[18]M. N. Kamalasanan, S. Chandra, P. C. Joshi, and A. Mansingh, Appl. Phys. Lett. **59**, 3547 (1991).
[19]V. D. Cammilleri, V. Yam, F. Fossard, C. Renard, D. Bouchier, P. F. Fazzini, L. Ortolani, F. Houdellier, and M. Hytch, Appl. Phys. Lett. **93**, 043110 (2008).
[20]H. Marchand, X. Wu, J. Ibbetson, P. Fini, P. Kozodoy, S. Keller, J. Speck, S. DenBaars, and U. Mashra, Appl. Phys. Lett. **73**, 747 (1998).
[21]A. Usui, H. Sunakawa, A. Sakai, and A. Yamaguchi, Jpn. J. Appl. Phys., Part 2 **36**, L899 (1997).
[22]S. Nakamura, M. Senoh, S. Nagahama, N. Iwasa, T. Yamada, T. Matsushita, H. Kiyoku, Y. Sugimoto, T. Kozaki, H. Umemoto, M. Sano, and K. Chocho, Jpn. J. Appl. Phys., Part 2 **36**, L1568 (1997).
[23]A. Nayfeh, C. O. Chui, and K. C. Saraswat, Appl. Phys. Lett. **85**, 2815 (2004).
[24]J.-S. Park, J. Bai, M. Curtin, B. Adekore, M. Carroll, and A. Lochtefeld, Appl. Phys. Lett. **90**, 052113 (2007).
[25]S. Kobayashi, M. Cheng, A. Kohlhase, T. Sato, J. Murota, and N. Mikoshiba, J. Cryst. Growth **99**, 259 (1990).
[26]H. Luan, D. Lim, K. Lee, K. Chen, J. Sandland, K. Wada, and L. Kimerling, Appl. Phys. Lett. **75**, 2909 (1999).
[27]A. K. Okyay, A. M. Nayfeh, T. Yonehara, A. Marshall, P. C. McIntyre, and K. C. Saraswat, Opt. Lett. **31**, 2565 (2006).